ABSTRACT OF DISCLOSURE

A fault tolerant computer includes a plurality of CPU modules that process the same instruction string while maintaining clock synchronization; and a plurality of I/O modules each having a plurality of device controllers executing input/output control processing for a device. A transaction synchronization controller, which checks if the sequences of I/O transactions issued from the plurality of CPU modules match, is provided in each device controller. If the sequences of I/O transactions issued from the plurality of CPU modules to each device controller match, a judgment is made that an out-of-synchronization condition is not caused.